

Appl No. 10/716,159  
Amdt. dated April 13, 2006  
Reply to Office action of January 13, 2006

### REMARKS/ARGUMENTS

Applicant would like to acknowledge, with thanks, the Office Action mailed 01/13/2006. This amendment and response is responsive to the Office Action mailed 01/13/2006. Claims 1, 8, 13, 16, 21 and 25 have been amended to more particularly point out and distinctly claim aspects of the present invention.

### **REJECTIONS UNDER 35 U.S.C. 102**

Claims 1-25 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No.20030172261 to Lee (*hereinafter* Lee). For reasons that will now be set forth, claims 1-25, as currently amended, are not anticipated by Lee.

By way of review, an aspect of the present invention is that a non-addressable memory such as a flash NAND operates in either a sequential mode or in a normal mode. Sequential mode is initiated responsive to an external signal being applied. A predetermined address is loaded into the internal register of the memory and data is serially sent sequentially starting from the predetermined address. Upon completion of transferring data in the sequential mode, the memory device switches to its normal operating state.

Claims 1, 8, 13, 16, 21 and 25, as currently amended, recite that a non-addressable memory (e.g. a flash NAND) upon receipt of a special instruction (e.g. a boot code) loads a predetermined address (e.g. the beginning of a boot code) into its internal register and then sequentially (serially) outputs data (e.g. boot instructions) beginning at the predetermined address. Upon completion of serially outputting the data, the memory switches to its normal operating mode.

By contrast, Lee is for a system and method for booting a computer using a NAND flash memory, where the boot code is transferred to a RAM for execution by the CPU (Abstract; ¶ 0010, 0047, 0049, 0052). The CPU then reads the boot code from the RAM (¶ 0010, 0047, 0049, 0052). Moreover, Lee only discloses that the NAND interface transfers data in block units (¶ 0007). Thus, Lee does not disclose a non-addressable memory capable of switching to a sequential mode to output a sequence of data and upon completion switching to a normal mode

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of operation. Furthermore, Lee does not teach that a pre-selected address for the beginning of the sequence is loaded into a register within the memory for outputting.

Claims 2-7, 9-12, 14-15, 17-20 and 22-24 directly depend from claim 1, 8, 13, 16, and 21 respectively, and therefore contain each and every element of claims 1, 8, 13, 16 and 21 respectively. Therefore, for reasons already set forth for claims 1, 8, 13, 16, 21 and 25; claims 2-7, 9-12, 14-15, 17-20 and 22-24 are also not anticipated by Lee.

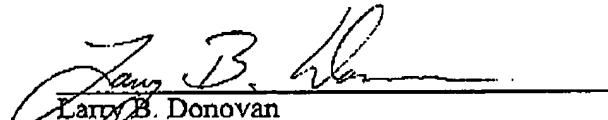
### CONCLUSION

For the reasons just set forth, it is asserted that the claims of the application are distinguished from the cited prior art. Therefore, a Notice of Allowance is earnestly solicited. If there are any fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. 64272/00001.

Respectfully submitted,

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Date: April 13, 2006

  
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